CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a first plurality of M number of conductors;

a second plurality of k sets of N number of conductors (k x N number of conductors); and

a switching network (SN), wherein M is at least k + N, where k is at least two and N is at least two;

wherein the SN comprises:

a plurality of switches;

a third plurality of I0 number of conductors, including N0 sets of $I0_i$ number of conductors for i = [1-N0], wherein N0 is at least two, N is at least N0, I0 is at least equal to M and between M and (k x N) when M is less than (k x N);

any two conductors of the first plurality of M number of conductors to selectively couple to at least two different conductors selected each from at least two different $I0_p$ number of conductors and $I0_q$ number of conductors, respectively, for p, q =[1-N0] through the plurality of switches without requiring traversal of another conductor;

a first conductor of said at least two different conductors to selectively couple to a first set of at most (k x (M/N0)) number of conductors through the SN,

wherein the first set of at most (k x (M/N0)) number of conductors has at most (M/N0) number of conductors from each of the k sets of N number of conductors; and

a second conductor of the at least two different conductors to selectively couple to a second set of at most (k x (M/N0)) number of conductors through the SN, wherein the second set of at most (k x (M/N0)) number of conductors has at most (M/N0) number of conductors, different from the first set of at most (k x (M/N0)) number of conductors, from each of the k sets of N number of conductors.

2. The integrated circuit of claim 1, each conductor of the $I0_i$ number of conductors to selectively couple k number of conductors through the SN without requiring traversal of another conductor.

3. The integrated circuit of claim 2, wherein the $I0_i$ number is at most a larger of (k x N/N0) number and (M/N0) number, and wherein the plurality of switches is at least [(M-N+1) x N + M x k] number of switches and at most M x (k + N) number of switches.

4. The integrated circuit of claim 2, further comprising k number of programmable logic cells, each of the k number of programmable logic cells having N number of input conductors, wherein each of the k number of conductors corresponds to one conductor of the N number of input conductors of the k number of programmable logic cells.

5. The integrated circuit of claim 1, where M is equals R x (k x N), wherein R is at least 0.5 and at most 1.0.

6. The integrated of claim 1, further comprising:

a fourth plurality of $I1_i$ number of conductors to selectively couple the $I0_i$ number of conductors, wherein the $I1_i$ number of conductors comprise N1 groups of $I1_{ij}$ number of conductors for j =[1-N1] where N1 is at least two, wherein

any two conductors of the $I0_i$ number of conductors to selectively couple to two different conductors of the $I1_i$ number of conductors through the plurality of switches without requiring traversal of another conductor, wherein a third conductor of the two different conductors is from $I1_{ir}$ number of conductors and a fourth conductor of the two different conductors is from $I1_{is}$ number of conductors and the number r is different from the number s for r, s = [1-N1];

the third conductor to selectively couple a third set of at most (k x (M/(N0xN1))) number of conductors from the k sets of N number of conductors through the SN, wherein the third set of at most (k x (M/(N0xN1))) number of conductors has at most (M/(N0xN1)) number of conductors from each of the k sets of N number of conductors; and

the fourth conductor to selectively couple a fourth set of at most (k x (M/(N0xN1))) number of conductors from the k sets of N number of conductors through

the SN, wherein the fourth set of at most (k x (M/(N0xN1))) number of conductors has at most (M/(N0xN1)) number of conductors, different from the third set of at most (k x (M/(N0xN1))) number of conductors, from each of the k sets of N number of conductors.

7. The integrated circuit of claim 6, wherein each conductor of the $I1_{ij}$ number of conductors selectively couples k number of conductors through the SN without requiring traversal of another conductor.

8. The integrated circuit of claim 7, further comprising k number of programmable logic cells, each of the k number of programmable logic cells having N input conductors, wherein each of the k number of conductors corresponds to one conductor of said N number of input conductors of the k number of programmable logic cells.

9. The integrated circuit of claim 7, wherein the $I1_{ij}$ number is at most the larger of (k x N/(N0xN1)) number and (M/(N0xN1)) number and the plurality of switches are comprised of at most [M x (N0+N1+k)] number of switches.

10. The integrated circuit of claim 1, wherein each of the plurality of switches is comprised of at least a program controlled passgate.

11. The integrated circuit of claim 1, wherein each of the plurality of switches is comprised of at least a program controlled drivers/receivers.

12. The integrated circuit of claim 1, wherein the plurality of switches are comprised of at least one of program controlled passgates and program controlled drivers/receivers.

13. The integrated circuit of claim 1, wherein one of the plurality of switches has a program controlled on state and off state.

14. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating memory devices.

15. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating non-volatile memory devices.

16. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating fuse devices.

17. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating anti-fuse devices.

18. The integrated circuit of claim 1, wherein the integrated circuit is implemented using process technology incorporating Ferro-electric devices.

19. The integrated circuit of claim 1, wherein M is determined by R x (k x N), where R is at least 0.5 and at most 1.0.

20. A method of connectivity in an integrated circuit comprising a first plurality of M number of conductors, a second plurality of k sets of N number of conductors (k x N number of conductors), and a switching network (SN) wherein M is at least k + N, where k is at least two and N is at least two, wherein the SN comprises a plurality of switches and a third plurality of I0 number of conductors, including N0 sets of $I0_i$ number of conductors for i = [1-N0], wherein N0 is at least two, N is at least N0, I0 is at least equal to M and between M and (k x N) when M is less than (k x N), wherein the method comprises:

selectively coupling any two conductors of the first plurality of M number of conductors to at least two different conductors selected each from at least two different $I0_p$ number of conductors and $I0_q$ number of conductors, respectively, for p, q =[1-N0] through the plurality of switches without requiring traversal of another conductor;

selectively coupling a first conductor of said at least two different conductors to a first set of at most (k x (M/N0)) number of conductors through the SN, wherein the first set of at most (k x (M/N0)) number of conductors has at most (M/N0) number of conductors from each of the k sets of N number of conductors; and

selectively coupling a second conductor of the at least two different conductors to a second set of at most (k x (M/N0)) number of conductors through the SN, wherein the second set of at most (k x (M/N0)) number of conductors has at most (M/N0) number of

conductors, different from the first set of at most (k x (M/N0)) number of conductors, from each of the k sets of N number of conductors.

21. The method of claim 20, further comprising selectively coupling each conductor of the $I0_i$ number of conductors to k number of conductors through the SN without requiring traversal of another conductor.

22. The method of claim 21, wherein the $I0_i$ number of conductors is at most a larger of (k x N/N0) number and (M/N0) number, and wherein the plurality of switches is at least [(M-N+1) x N + M x k] number of switches and at most M x (k + N) number of switches.

23. The method of claim 21, further comprising k number of programmable logic cells, each of the k number of programmable logic cells having N number of input conductors, wherein each of the k number of conductors corresponds to one conductor of the N number of input conductors of the k number of programmable logic cells.

24. The method of claim 20, where M equals R x (k x N), wherein R is at least 0.5 and at most 1.0.

25. The method of claim 20, further comprising:

selectively coupling a fourth plurality of $I1_i$ number of conductors to the $I0_i$ number of conductors, wherein the $I1_i$ number of conductors comprise N1 groups of $I1_{ij}$ number of conductors for j =[1-N1] where N1 is at least two;

selectively coupling any two conductors of the $I0_i$ number of conductors to two different conductors of the $I1_i$ number of conductors through the plurality of switches without requiring traversal of another conductor, wherein a third conductor of the two different conductors is from $I1_{ir}$ number of conductors and a fourth conductor of the two different conductors is from $I1_{is}$ number of conductors and the r is different from the s for r, s = [1-N1];

selectively coupling the third conductor to a third set of at most (k x (M/(N0xN1))) number of conductors from the k sets of N number of conductors through the SN, wherein the third set of at most (k x (M/(N0xN1))) number of conductors has at most (M/(N0xN1)) number of conductors from each of the k sets of N number of conductors; and

selectively coupling the fourth conductor to a fourth set of at most (k x (M/(N0xN1))) number of conductors from the k sets of N number of conductors through the SN, wherein the fourth set of at most (k x (M/(N0xN1))) number of conductors has at most (M/(N0xN1)) number of conductors, different from the third set of at most (k x (M/(N0xN1))) number of conductors, from each of the k sets of N number of conductors.

26. The method of claim 25, further comprising selectively coupling each conductor of the $I1_{ij}$ number of conductors to k number of conductors without requiring traversal of another conductor.

27. The method of claim 26, further comprising k number of programmable logic cells, each of the k number of programmable logic cells having N number of input conductors, wherein each of the k number of conductors corresponds to one conductor of the N number of input conductors of the k number of programmable logic cells.

28. The method of claim 26, wherein the $I1_{ij}$ number is at most the larger of (k x N/(N0xN1)) number and (M/(N0xN1)) number and the plurality of switches comprises at most [M x (N0+N1+k)] number of switches.